REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 32 to clarify structure having the insulating supporting member and the plural sets of wirings, and to recite that the external connection terminals provide a cap on the openings, and have further amended claim 2 to correct the spelling of "semiconductor" in the last line of page 2.

In addition, Applicants are adding new claims 42-53 to the application. Claim 42, dependent on claim 32, recites that the external connection terminals completely block the openings; and claim 44 and 46, each dependent on claim 32, respectively recites that the plural sets of wirings are provided on a surface of the insulating support member, and recites that the semiconductor device mounting region is provided at the one side of the insulating support member. Claim 50, dependent on claim 32, recites that the openings extend completely through the insulating support member. Claim 48 expressly sets forth subject matter expressly recited in claim 42, but is dependent on claim 46; and claim 49 expressly recites subject matter expressly set forth in claim 44, but is dependent on claim 46. Claim 51 expressly recites subject matter expressly set forth in claim 46, but is dependent on claim 50. Claims 43, 45, 47, 52 and 53 recite subject matter expressly set forth in claim 37, but are dependent respectively on claims 42, 44, 46, 51 and 50.

In connection with amendments to previously considered claims, and in connection with the newly added claims, note, for example, Figs. 17a-17d of Applicants' disclosure, and the corresponding description on pages 36-41, of Applicants' specification.

The objection to claim 32 as set forth in the second paragraph on page 2 of the Office Action mailed March 7, 2006, is moot, in view of present amendments to claim 32 correcting the spelling of "semiconductor" in line 19 thereof.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the prior art applied by the Examiner in rejecting claims in the Office Action mailed March 7, 2006, that is, the teachings of the U.S. patents to Ackermann, et al., No. 4,975,765, to Yamaguchi, No. 5,250,470, to Enomoto, et al., No. 5,175,060, to Lumbard, et al., No. 4,890,383, and to Pennisi, et al., No. 5,313,365, under the provision of 35 USC 103.

It is respectfully submitted that the references as applied by the Examiner would have neither taught nor would have suggested such a substrate for semiconductor packages, or such a semiconductor package formed utilizing such substrate, as in the present claims, the substrate having an insulating supporting member and plural sets of wirings formed on one side of this insulating supporting member, and wherein, inter alia, openings are provided in the insulating supporting member at points where external connection terminals, of the wirings, are formed, the openings reaching the external connection terminals, the external connection terminals providing a cap on these openings, with plural sets of the semiconductor device mounting and the semiconductor package regions being formed on the insulating supporting member, and wherein the wire bonding terminals are provided in the semiconductor package region and the external connection terminals are provided only within the semiconductor device mounting region. See claim 32. Note also claim 37, reciting the package produced by a method including use of this substrate.

In addition, it is respectfully submitted that these applied references would have neither disclosed nor would have suggested such substrate or such semiconductor package as in the present claims, having features as discussed previously in connection with claims 32 and 37, and, additionally, wherein the plural sets of wirings are formed only on the one side of the insulating supporting member (see claim 41); and/or wherein the external connection terminals completely block the openings (see claim 42; note also claim 48); and/or wherein the plural sets of wirings are provided on a surface of the insulating support member (see claims 44 and 49); and/or wherein the openings extend completely through the insulating supporting member (see claim 50); and/or wherein the semiconductor device mounting region is provided at the one side of the insulating support member (see claims 46 and 51); and/or the semiconductor package formed utilizing the substrates respectively of claims 42, 44, 46, 51 and 50 (see claims 43, 45, 47, 52 and 53, respectively).

In addition, it is respectfully submitted that the teachings of these applied references would have neither disclosed nor would have suggested such a substrate for semiconductor packages as in the present claims, having features as discussed previously in connection with claim 32, and additionally including, inter alia, wherein the wire-bonding terminals include a nickel layer and a gold plate layer on its surface (see claim 35); and/or wherein the external connection terminals are arranged in a grid pattern at positions corresponding to a semiconductor device mounting region of the substrate (see claim 36).

By providing external connection terminals that are a cap on the openings, as in the present claims, particularly with further definition of such cap and wirings as in other claims, leakage of adhesive and/or sealing resin through the openings, during

fabrication of the semiconductor package, can be avoided. Note, for example, Figs. 17c-17f, of Applicants' original disclosure. See also, for example, Figs. 6c-6e of Applicants' original disclosure.

Ackermann, et al. discloses a highly integrated circuit, especially for a multi-chip module, in which there are provided inside the mounting area in the substrate through-metalized through-holes which conductively connect the top side of the substrate to its underside, with underside contact areas in the form of bumps. The through-holes are arranged with a grid spacing which is considerably larger than a first grid spacing, and at least on the top side of the substrate conductor tracks extend to the through-holes starting from first connecting areas. See column 3, lines 40-52. Note also column 1, lines 9-27, and column 3, lines 7-17. See also the paragraph bridging columns 6 and 7 of Ackermann, et al., as well as column 7, lines 13-18.

It is respectfully submitted that Ackermann, et al. discloses through-holes, with, e.g., plating covering the peripheral surfaces of the through-holes. It is respectfully submitted that the disclosure of Ackermann, et al. would have neither taught nor would have suggested such external connection terminals as in the present claims, providing a cap on the openings, and, in particular, completely blocking the openings, and advantages thereof.

As a comparison of the structure of Ackermann, et al. and the presently claimed subject matter including the external connection terminals, attention is respectfully directed to the enclosed Reference Drawing, showing, e.g., the subject matter of the presently claimed subject matter, illustrated by (but not limited to) structure seen in Fig. 17c, of the above-identified application, as compared with through-hole structure as in Ackermann, et al. As can be appreciated, Ackermann,

et al. would have neither taught nor would have suggested such external connection terminals acting as a cap of the openings, in particular completely blocking such openings, and advantages achieved thereby.

It is emphasized that the through-holes of Ackermann, et al. are formed in the substrate to connect upper and lower surfaces of the substrates, with a conductive connection via the through-hole electrically connecting such upper and lower surfaces. In contrast, it is respectfully submitted that the openings as in claim 32 are not through-holes. Wirings are formed on one side of the substrate, and external connection terminals are part of such wirings. The external connection terminals are formed beforehand on the surface of the substrate.

Accordingly, the structure of Ackermann, et al., including the though-holes, is different structurally from the subject matter of claim 32.

It is respectfully submitted that the additional teachings of Yamaguchi would not have rectified the deficiencies of Ackermann, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Yamaguchi discloses a semiconductor device of a thin package type used in integrated circuit (IC) cards or the like, the device including a semiconductor element having pads; a supporting member having a mount region on which the semiconductor element is mounted; a plurality of leads which are pattern-formed on the supporting member, and which have first ends positioned near the mount region and second ends; conductors for connecting the first ends of the leads to the pads of the semiconductor element; and sealing material for sealing at least the conductor and the semiconductor element, with the second ends of the leads being provided collectively at a region along the circumference of the supporting member, and

sealed by the sealing material. See column 2, lines 43-57. Note also column 3, lines 20-24; and column 5, lines 7-20.

Even assuming, arguendo, that the teachings of Yamaguchi were properly combinable with the teachings of Ackermann, et al., the combined teachings would have neither disclosed nor would have suggested such structure as in the present claims, including, inter alia, the openings provided in the insulating supporting member at points where the external connection terminals are formed, with the external connection terminals providing a cap on the openings, and advantages thereof as discussed in the foregoing; and/or the other features of the present invention as in the present claims, and discussed previously.

With respect to claim 35, it is respectfully submitted that the additional teachings of Enomoto, et al. would not have rectified the deficiencies of the combined teachings of Ackerman, et al. and of Yamaguchi, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Enomoto, et al. discloses a semiconductor-mounting substrate having a desired conductor circuit directly formed onto a lead frame through an insulating layer, and wherein an adhesive layer is arranged on at least a part of the lead frame directly or indirectly through the insulating layer, the conductor circuit being formed by an additive process through the adhesive layer, the conductor circuit being connected to leads of the lead frame by plating. See column 2, lines 30-38. Note also column 4, lines 1-8. This patent discloses that as for the metal to be used in electroless or electro-plating, it is desirable to use gold, silver, copper, nickel or the like as well as an alloy thereof; and that, particularly, when the semiconductor part is

connected to the conductor circuit through a gold wire by the wire bonding method, a combination of gold/nickel/copper is preferably used. See column 6, lines 16-24.

Even assuming, arguendo, that the teachings of Enomoto, et al. were properly combinable with the teachings of Ackermann, et al. and Yamaguchi, it is respectfully submitted that such teachings would have neither disclosed nor would have suggested the presently claimed substrate or package produced using such substrate, including, inter alia, the external connection terminal providing a cap on the openings provided in the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals, and advantages thereof; and/or other features of the present invention as discussed previously, and advantages thereof.

It is respectfully submitted that, with respect to the subject matter of claim 37, the additional teachings of Lumbard, et al and of Pennisi, et al., even if properly combinable with the teachings of Ackermann, et al. and Yamaguchi, would not have rectified the deficiencies of Ackermann, et al. and of Yamaguchi, as discussed previously, such that the presently claimed invention as whole would have been obvious to one of ordinary skill in the art.

Lumbard, et al. discloses electro-optical displays and other modular compact components, having an electrically insulating, generally planar substrate with two opposing major surfaces, the first of the two major surfaces including a plurality of land areas for receiving devices to be mounted thereon and a plurality of connection paths, and the second of the two major surfaces including a plurality of terminal pads serving as external terminals for mounted devices, with plated through-holes for providing electrical connection between some of the external terminals to the land

areas and between the remaining external terminals to the connection paths. Note, in particular, column 2, lines 1-32.

Pennisi, et al. discloses electronic packages for semiconductor devices and integrated circuits, especially encapsulation of semiconductors directly attached to a circuit substrate, wherein a printed circuit board with a metal circuit pattern is provided on one side thereof; one or more semiconductor devices are attached to the printed circuit board with an adhesive, and covered by a glob top encapsulant; and the glob top encapsulant also covers portions of the printed circuit board surface, the printed circuit board, adhesive and encapsulant all being made from the same type of resin. See column 2, lines 22-30.

It is emphasized that Lumbard, et al. discloses plated through-holes. It is respectfully submitted that the structure formed is similar to that of Ackermann, et al., and would include through-holes with metal plating on peripheral surfaces of such holes, as seen in the enclosed Reference Drawing in connection with Fig. 3C of Ackermann, et al. Even assuming, arguendo that the teachings of Lumbard and Pennisi, et al. were properly combinable with the teachings of Ackermann, et al. and of Yamaguchi, as applied by the Examiner, such combined teachings would have neither disclosed nor would have suggested the presently claimed substrate or package formed utilizing such substrate, including, inter alia, the openings provided at the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals, with the external connection terminals providing a cap on the openings, and advantages thereof; and/or other features of the present invention, in combination therewith, including the semiconductor package produced, and advantages thereof.

The contention by the Examiner in the paragraph bridging pages 2 and 3 of the Office Action mailed March 7, 2006, that Ackermann, et al. discloses openings (18 in Fig. 3C) provided in the insulating supporting member at points where the external connection terminals are formed, reaching the external connection terminals, is respectfully traversed, particularly insofar as applicable to the claims as presently amended. Thus, as can be seen in the enclosed Reference Drawing, Ackermann, et al. discloses through-holes with metal plated on surfaces thereof, the metal extending via the through-hole on opposed surfaces of the substrate. Such structure is different from, and would have neither taught nor would have suggested, the openings as in the present claims at points where the external connection terminals are formed, reaching the external connection terminals; and, in particular, wherein the external connection terminals provide a cap on the openings, and/or completely block the openings.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently pending in the above-identified application are respectfully requested.

Applicants request any shortage in fees due in connection with the filing of this paper be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 648.43481CC4), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
William I. Solomon
Reg. No. 28,565

Attachment: Reference Drawing (1 pg.)

WIS/ksh
1300 N. Seventeenth Street
Suite 1800
Arlington, VA 22209
Tel: 703-312-6600
Fax: 703-312-6666